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A Philosophical Unification of Arithmetics and Electronic Machine.

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A PHILOSOPHICAL UNIFICATION OF ARITHMETICS AND ELECTRONIC MACHINE.

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Abstract. This paper investigates the unification of arithmetics by first treating the theorem of One-arithmetical equality with machine philosophy in electronic domain. The theorem is made up of 5 parts just like the computer units. Computer is an electronic machine that has programs for reading, writing and storing in an electronic domain. There are nine(9) questions concerning "What", "Who", "Which", "Who-ness", "Which-ness" and "Where-ness" of the One-arithmetical equality and their proof answers in machine concepts. Theorem (4) of the One-arithmetical equality is described in this paper as Division Equality Theorem and it I-V characteristics in memristor array design in memory device. A coin analogy is employed in the teaching of H-O-N system. This paper investigated the person who is involved in the provision of product information and the storage of results in an electronic machine memory – Computer Memory. It also put forward ways to name and study things as encountered in a computer field matter. The phrase "Who-ness to who" is a call to study a thing encountered- Central Processor Unit(CPU), Arithmetic Logic Unit(ALU), Memory Unit(MU), Datapath and Control Units(DCU). The discovery of Rightus Equalus is verbally proved in this machine paper. The list of claims are provided in the final section of this paper.

Keywords. signs, arithmetical, Hon system, division, equality, unification, proof, mathematical; machine; electronic machine; number system; parts.

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1 INTRODCUTION

This section starts with the theorem of One-Arithmetical Equality. In the One-Arithmetical Equality theorem, I look at the multiplication of ones, addition of ones, difference of ones, division of ones and equality of ones. The first principles of proving 1+1=2 is philosophical as mathematical and [2] is one that build on themselves a chain of reasoning.

Theorem (One-Arithmetical Equality):

- 1 x 1 = 1
- 1 + 1 = 2
- 1 - 1 = 0
- 1 / 1 = 1
- 1 =1

The unification of arithmetics and electronic machine from One-arith theorem will be elemented on the current operation of computer today. Elementing the theorem shows chain of reasonings for the electronic machine in general.

- Which-ness of 1x1?
- What is 1x1?
- Which-ness to what is 1x1?
- Where-ness to what is 1x1?
- Who-ness to what is 1x1?
- Who is 1x1?
- Who-ness to who is 1x1?
- What is 1-1?
- Where-ness to what is 1-1?
- What, which, where and who (who-ness) of electronic machine in involved in One-Arithmetical Theorem.

2 ARITHMETIC ELECTRONICS

Let us now look at answers to these question.

The electronic calculation of numbers is performed in the ALU and information transfer to/from the storage memory in a Von-Neumann system.

Answers : Let us proof[1] the questions above:

- The which-ness of *1x1* is *1/1* from theorem (1)

  1 x 1 = 1 / 1.

  1 / 1 is the division of one by itself.

  The concept of division of one by itself is envisaged as memristor array of a memory device. The which-ness of the division of a machine is know as impossible but dimensional array of memristor components is which-ness to the storage of the information.

  1 is a true binary information.

  x is a crossbar of memristor array at the diagonals of a dimensional arrray components.

  / is a diagonbar of memristor array at the right diagonal of dimensional array components.

  = is a read-line or write-line of memristor array components in a memory device.

  1 is a self-truth of binary information.

  1=1 is either a read or write line of communication each on a different line of path.

Information storage on the electronic machine is a combination of 0(zeros) and 1(ones). This is the binary format of the electronic domain of -/+ 5v of power of source. This means a less than 5v will represent a zero unary format of information whiles 5v electronic domain represents a a one unary format. The combination of 1-unary and 0-unary is a binary format of information storage. The information can be classified as data or image or voice. The informatics of data, voice and image information are different in only storage

manipulation. Generally, it is a bit/byte field of information from the write of a program. Each kind of information is manipulated in a different way to differentiate between the informations. Byte is an information of 8 bits in an electronic device like memory.

The equality of read or write is symbolized as an equal sign of arithmetic. Why 1=1? The first is visionally to see that there is a number at both sides of the equality meaning to the same number. Here, it will be a machine theory to have something different that one and itself. Again, it will require that a write of 1-unary datum on the equal readline should show the same even after electronic domain conversion. Simply put, a write cause of 1 datum will effect a read of 1-datum on any electronic display in any real world. This is so today even though this document is written on an electronic machine. The essence of knowledge in electronic machine philosophy is the essential of study and investigation.

- *1 x 1* is the multiplication of one by itself from theorem (1)

  1 x 1 = 1.

  This means the result of the multiplication of one by itself is a product of the number, one ie The result is itself, one. In electronic domain, a multiplication of 1 by 1 is not simply like multiplying a 5v by 5v in electronic domain. This will require a combinational circuit called *multiplier* (digital or analogy device) in ALU to achieve the results even before storage in memeory.

  1 is a unary information as 5v.

  x is a digital multiplier, electronic device.

  = indicates a communication of result to the memory to enable read or write at the same time or not. There are two modes of system

execution- User and Kernel Mode. This is possible as user writes and kernel unit reads in an operating system and vice versa. _ line is bit lines of the memristor corssbar array to read whiles – line is the word line to write.

1 is a bit of information in memory device. Misrepresentation can be more bits or a zero read in a nonvolatile memory logic.

- The which-ness to what is *1 x 1* needs that first the question of what is *1 x 1* answered.

  Trying to qualify 1 x 1 if theorem (1) gives that

  1 x 1 = 1.

  Then the result of *1 x 1* is known and if the result of 1 x 1 is not needed because of the knowledge of equality. The quality of the result is by having the sign of equality on the right hand side and not on the left hand side. The sign of quality for :

  (a) Right (R) Hand (H) Side (S): RHS

  for RHS of 1 x 1 = 1 results from the sign of equality.

  Hence (1 x 1) = 1. Therefore, the sign of quality of the result is "=*1*". This is called *one-assignment or equals_to_one.* Information transfer in the assignment of result to a memroy cell for easy retrieval is the sign of quality of information. Rightly, information is handed in three different approaches namely: *1T1M[4]* (Transistor-Memristor Array Approach), *1D1M[5]* (Diode-Memristor Array Approach) and *1S1M [6]* (One Selector-Memristor) to single-to-many(one-to-many) memory cell(s) in a memory device. A writing process of a memory

device can be described as a *Cell Assignment*[2] for ones or *Non-cell Assignment*[3] for zeros. A reading process of a memory device can be described as *Cell Equivalence*[4] for ones or *Non-cell equivalence*[5] for zeros.

Definition 1 [Electronic Information Transfer]

Information transfer in arithmetic machinery is now a process of multiple domaining of electrons transfer in Cell Assignment/Cell Equivalence or/and Non-cell Assignment /Non-cell Equivalence.

Definition 2 [Electronic Information Transfer]

Memory assignment is a combination of both write assignment process in ones and zeros.

Definition 3 [Electronic Information Transfer]

Memory Equivalence is a combination of both read equivalence process in ones and zeros.

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[2] Cell Assignment is a write process of information transfer into a memory cell of an electronic memory in ones only.

[3] Non-cell assignment is a write process of information transfer into a memory cell of an electronic memory in zeros only.

[4] Cell Equivalence is a read process of information transfer into a memory cell of an electronic memory in ones only.

[5] Non-cell Equivalence is a read process of information transfer into a memory cell of an electronic memory in ones only.

Assignment and Equivalence of quality information in Non-volatile memory is sign of quality information transfer in both read or write processes. Therefore, Quality Assignment demands a quality non-volatile memory in a Von-Neumann System for storage. Hence, Quality Equivalence supplys information from a non-volatile memory in a Von-Neumann system.

Assignment Information Transfer (AIT) in arithmetic machinery is a process of multiple domaining electrons in assignment to memory crossbar array. Assign of -/+ 5ev to a memory cell in crossbar array is a sign of zero or one electronic information. *Equivalence Information Transfer (EIT)* in arithmetic machinery is a process of multiple domaining valence electrons in equivalence to memory crossbar array. Equivalent current of -/+ 5ev from a memory cell in crossbar array is a value of 0 or 1 electronic information.

(b) Left (L) Hand (H) Side (S) : LHS

for LHS of 1 x 1 = 1, results from the sign of multiplication. Hence , 1 x 1 =1. Therefore, the sign of quality of the result is "*1x*". This is called *one-product* or *one_by_anynumber*.

Electronic machine or Computer is one product based on Von-Neumann machine or system with the capability to provide the unification of parts in quality information results. Electronic machine makes it business to perform electronic calculations on many fields of arithmetic namely addition, subtraction, division and multiplication.

Digital circuits in this machine creates the circuitry to undertake an electronic calculation. Here, it is important to note that the issue of address is to look at

electric circuits and circuit topologies of technical drawing a topology of the theorems above. Again, a look at the equivalent circuit of these topologies as lump element circuits- Resistors(R), Capacitors(C) and Inductors(L).

(c) The count of the alphabets "*right*" is 5. Then if

$$\underset{(1)}{1} \; \underset{(2)}{x} \; \underset{(3)}{1} \; \underset{(4)}{=} \; \underset{(5)}{1} \; (1)$$ RH- structure.

The equality theorem (1) provides a 5 -element count and the first is1 from the left-to-right count;

(A) Element 1 : 1

(B) Element 2 : x

(C) Element 3 : 1

(D) Element 4 : =

(E) Element 5 : 1

Therefore the count of alphabets "right" falls on the fifth element and that is one. Hence the RH-system gives the result. On the other hand , LHS The count of the alphabets "left" is 4.

The equality theorem can be a topological circuit with drawing lines for the arithmetic calculation in parts or whole to form a network topology for anynumber but focus on the One-Arith Theorems. From the circuit topology, an electric circuit equivalence can be made to assess I-V characteristics to electronic viability. The machine theory is that once each circuit has different I-V characteristics, it is possible to identify when 1 +1 =2 or 1 x 1 =1. Fabricating a circuit topology can be elemented as a resistor lump element and passing current through will give variant I-V characteristics measurement

to help identify each arithmetic circuit theorem. The two approaches are viable to successfully experimenting on the concepts drawn. RH-system circuit is realized if the topology is done from the right-handed side of the arithmetic. RH-system topology fabricated will result into an RH-system product.

Then if

$$\underset{(5)\ (4)\ (3)\ (2)\ (1)}{1\ \ x\ \ 1\ \ =\ \ 1\ (2)}$$ LH- structure.

The equality theorem (1) with it's 5-element count and the first being 1 from the right-to-left count;

(Ari) Element 1 : 1

(Bi) Element 2 : =

(Ci) Element 3 : 1

(Di) Element 4 : x

(Ei) Element 5 : 1.

Therefore, the count of the alphabets “left” falls on the 4 th element and that is x. Hence LH- system gives the product.

If 1 x (1 = 1)

then the equality theorem (v) gives

that 1 = 1 is a perfect quality product (PQP).

LH-system circuit is realized if the topology is done from the left-handed side of the arithmetic calculation. LH-system topology fabricated will result into an LH-system product. 1=1 network topology is a perfect quality system product.

This is because by applying the one-product on both sides of the PQP gives

(a)

$$
\begin{aligned}
&1 = 1 \\
&1 = 1 \ \ by \ \ 1x \\
&1 \ x \ 1 = 1 \ x \ 1 \\
&(1 \ x \ 1) = (1 \ x \ 1) \ \ Applying\, RH-system \\
\text{If} \quad &=1 \ \ = \ \ =1 \ \ Applying\, perfection \\
&1 = 1 \ \ = \ \ 1 = 1 \ \ Perfection\, Assignment\, , Theorem\ (5) \\
&(1=1) \ \ = \ \ (1=1) \, Applying\, RH-system \\
&1 \ \ = \ \ 1 \ \ PQP \\
&=1.
\end{aligned}
$$

This method is to be used to generate a complex board circuit. From the last result a topology for 1=1 can be reduced to =1 network topology to reduce fabrication time and all. But, there are about 9 processes generated to achieve same results. A summing amplification of each cascade of circuit topology can be from 1=1, then to 1x1=1x1, to (1x1)=(1x1) then to =1==1 to 1=1=1=1 then (1=1)=(1=1) again to 1=1 and finally =1. This creates a cascade circuit topology.

(b) If

$$1 = 1$$
$$1 = 1 \ \ by \ \ 1x$$
$$1 \ x \ 1 = 1 \ x \ 1$$
$$(1 \ x \ 1) = (1 \ x \ 1) \ \ Applying \ \ RH-system$$
$$(i) = 1 \ \ = \ \ = 1 \ \ Applying \ \ Assignment$$
$$(ii) = 1 \ \ (= =) \ 1 \ \ Applying \ \ Equivalence$$
$$(iii) = 1 \ \equiv \ 1 \ \ Applying \ \ perfection$$
$$(iv)(1 = 1) \ \equiv \ 1 \ \ Applying \ \ RH-system$$
$$(v) \ 1 \equiv 1.$$

1. This is called or read as equals_to_one is the double_assignment of one
2. This is read as the equals_to_one is the bracket double assignment of one.
3. This is read as the equals_to_one is the equivalent one.
4. This is read as the one_equals_to_one is equivalent_to_one.
5. This is lastly read as one is equivalent to one.

The which-ness to what is 1 x 1 is answered by RH- system. The RH-system gives a result from theorem (1) ; Therefore 1 x 1 = 1. This means RH-system results to an equals_to_one. From the theorems (4) and (5), the theorem (4) is the division of one by itself and results to an equals_to_one but theorem (5) is the equality of one to itself and do not result to any number except itself because of the missing operator.

If the result to what is *1 x1* is an equals_to_one and the theorem (4) gives

$$1 \ / \ 1 \ = 1$$

then the which-ness of what is 1 x 1 is a theorem which results to the equals_to_one with no missing operator. That theorem is theorem (4)

Characteristics of Division Equality Theorem

a. It has the sign of division.

b. It is arithmetical.

c. It has the divide operator.

d. It results to the equals_to_one and has the quality of one_assignment.

- The where-ness to what is *1 x 1* needs first the answer to what is *1 x 1*. Question (ii) has quality ,

  1 x 1 to be the multiplication of one by itself and it is a product of the number, one. The two hand systems are right and left hand systems. Right hand system lies to the right hand side whiles the left hand system also lies to the left hand side. The question can be put in another sense and that is where is the multiplication of one by itself. If this question is answered then the answer to the main question is the other side of the coin (This is because there are only two sides of a coin). So if one lies on the left hand side then the other is on the right hand side and vice versa. 1 x 1 lies on the left hand side. To the main question, what is *1 x1* is a product of the number, one and if *1 x 1* lies on the left hand side then the where-ness to what is 1 x 1 is qualified by design to lie on the right hand side.

Of course, to my own thinking there is a third side of the coin which is the wheel to show both sides. An analogy to the coin idea will show that there are three systems including:

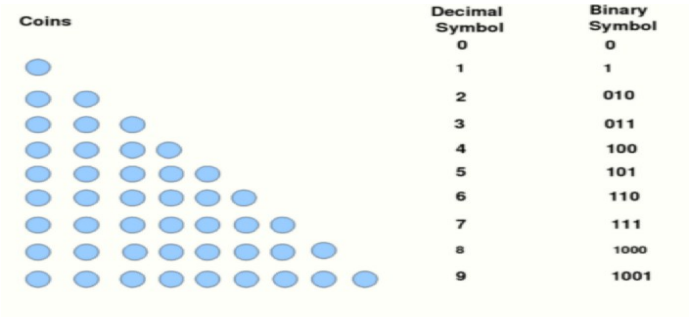
(i) Operator System or Field System

(ii) Hand System

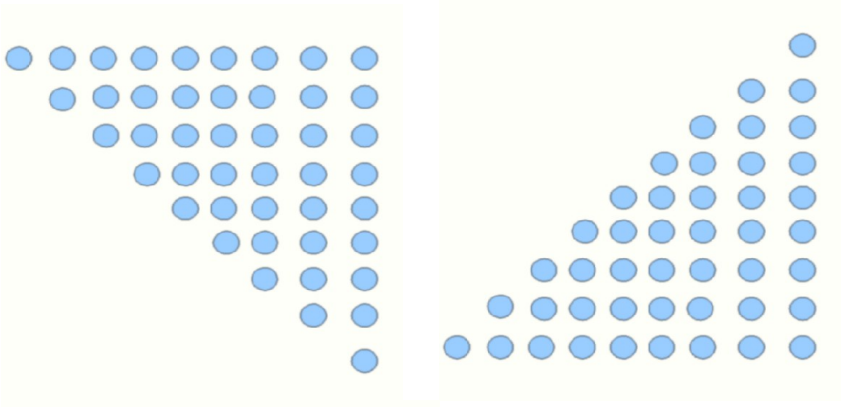
(iii) Number System.

It can be abbreviated as (H)and (O)perator (N)umber, HON. It is a Z_2 field system.

Z_2 field system on the number system is based on 0 to 9. It is topological envisaged as several coin dots possibly fabricated as a quantum dot system. The dot topological pattern is shown as below:

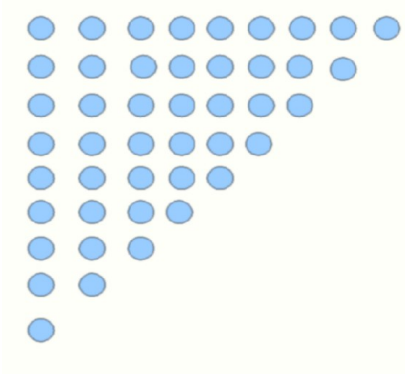


Non-Flip Coindots.



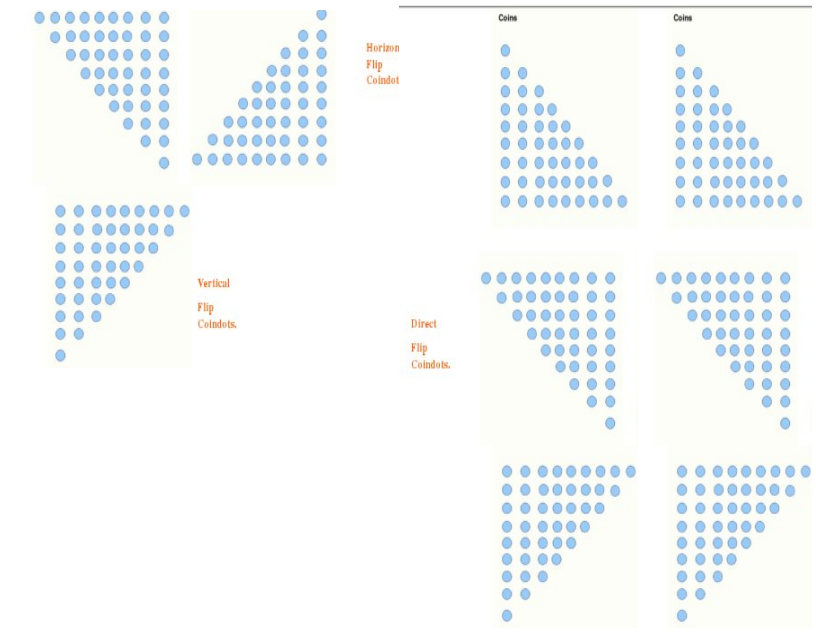
Direct Flip Coindots.

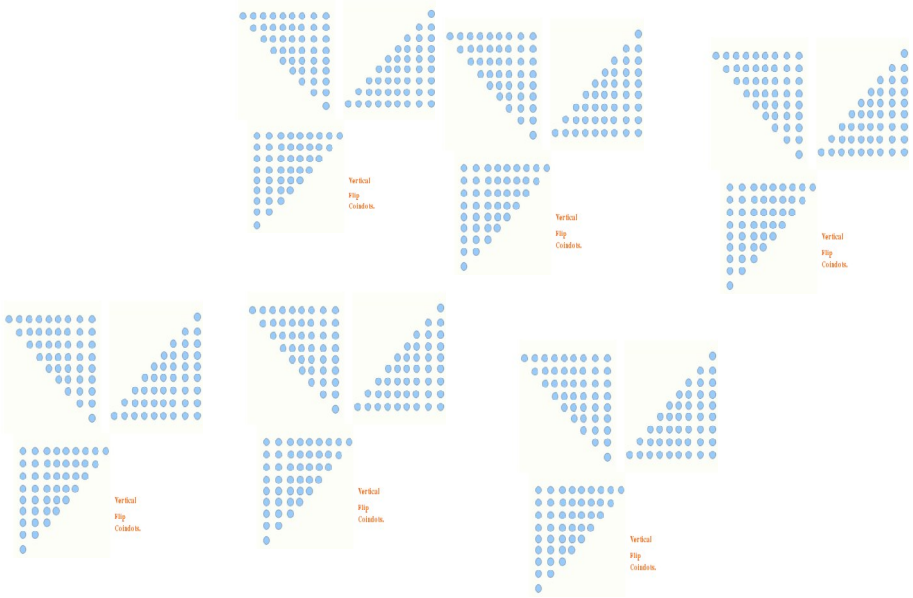
Horizontal Flip Coindots.



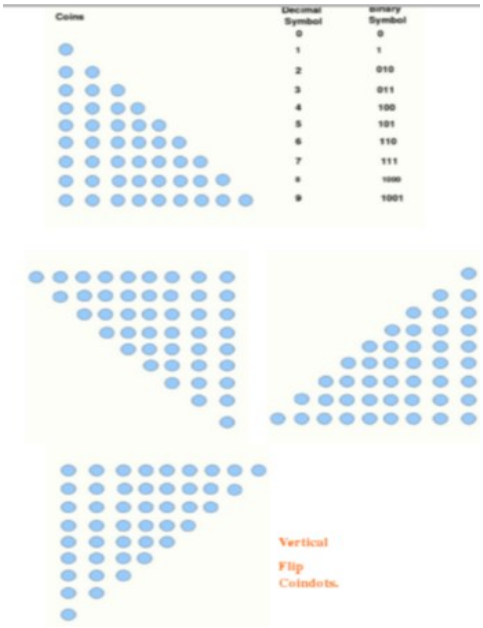
Vertical Flip Coindots.

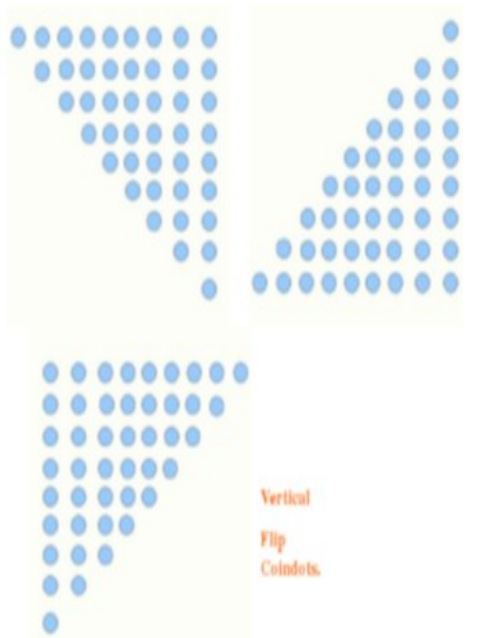
Arithmetronics: Arithmetic Electronics

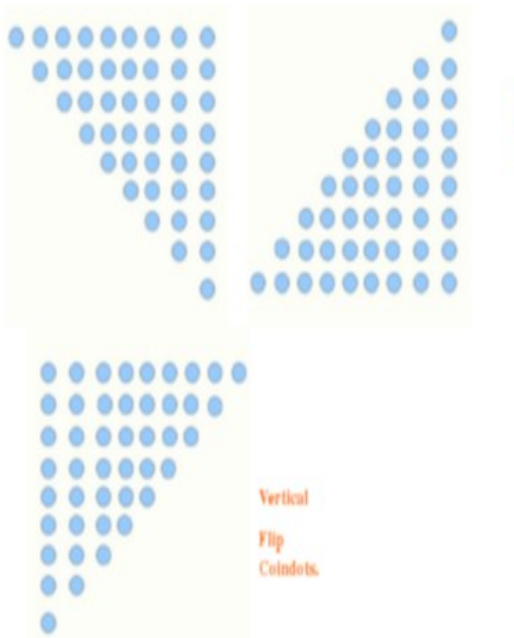




Arithmetronics: Arithmetic Electronics



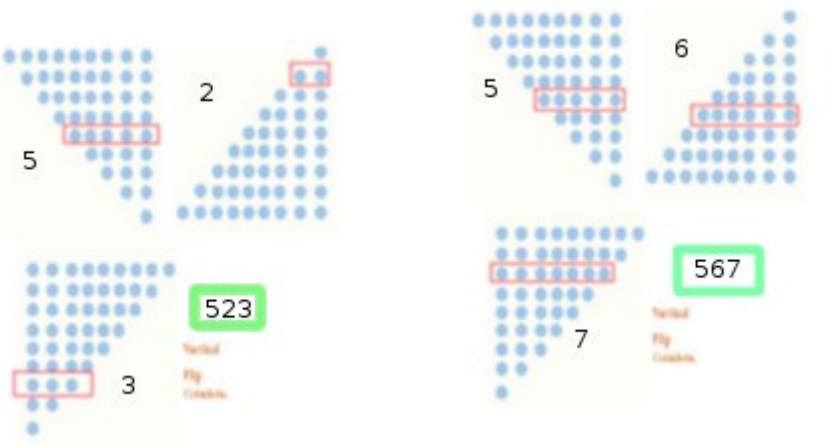




Z-field system on hand system will deal with switches in selection of numbers circuit. The concern here is dealing with order and repeation of numbers. This calls for an order circuit to select order in one number and a repeat circuit to handle repeation of numbers in one selection.

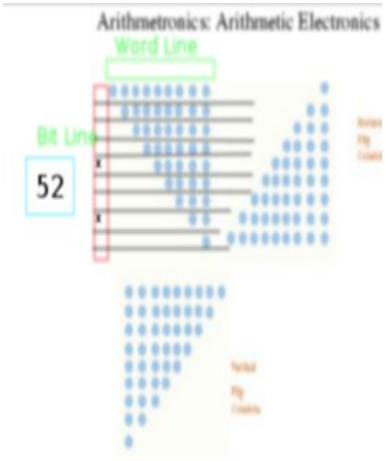
Z-field system on operator system will handle main operation of number formation, concatenation numbers, order arrangement, repeation sorting and more.

1S1N Approach: One Selector One Number

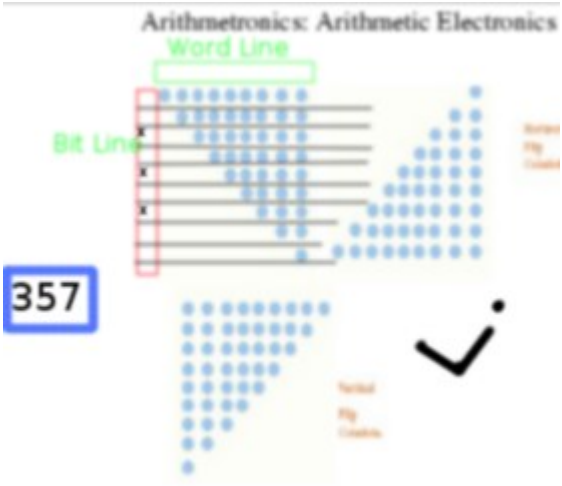


This is about selecting a dot grid system and so 5 digit number will require five grid number system. It is a top-down approach in selection of a number for each number system. Here, two number systems are described with red selection for digit and green display box. 523 and 567 number system is depicted to show implementation of system.

1M1N Approach: One Multiple One Number



This is about multiple selection with reverse circuit in generating numbers for a number system. Here, 52 is selected by switches by turning



it on with a switch corresponding to coindots number. 357 number is made but with reverse switch is turned on for reverse reading. This means instead of reading the first grid with 9 as the first read value, it is rather 1 which is the first read number in reverse circuit. Without turned on reverse switch, it will read 753 instead.

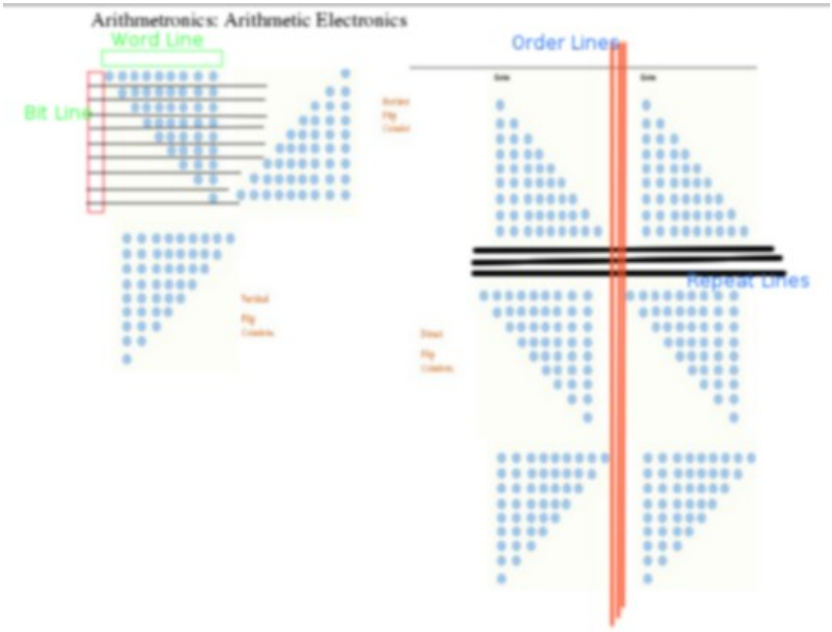
- The who-ness to what is 1 x1 needs the results of the multiplication of one by itself answered. It is a product of the number, one as depicted in the answer to question (ii). From the answer provided in (iii), the

quality of the result is equals_to_one. The question "*What is 1 x ?*" is equals_to_one and to the main question "*Who-ness to what is 1 x1* ";

Who means which person is involved in the provision of product information. What is the name? The who-ness is asking of the person who will be adding the result information or the person who knows of "*What is 1 x1 ?*" in the involvement of something – the multiplication of one by itself. The origin of the theorem (1) is deceptively subtle issue but the discover ways are from the fields of algebra. The fields of algebra are based on rules that define them. It just works as it is for nay fields and no matter the encounter field - We need never prove it. The modus operandi of the algebraist are to name and study the things we named. If we encounter the field of 1 x 1 matter, then name of power that will be adding the result information is Equalus Unitus. Then, Equalus Unitus knows of "*What is 1 x 1?*" and rules that define it. Equalus Unitus is involved in the provision of product information if we encounter the field of 1 x 1 matter. We need never prove it because Equalus Unitus obeys the arithmetic rules and it works just as it is for any field. The modus operandi of the algebraist just have call it and the answer is provided.

E1M1N Approach: Enhanced One Multiple One Number

This is an enhanced version of one multiple one number. There is a consideration of order and repeat in number generation. There is no reverse circuit in this design.



The red lines indicate an ordering of numbers whiles the black lines indicate a repeation of numbers. A 3/6-digit with each repeated grid number gives a total of 3 to 6 digits in just one read for a number system.

- If we encounter the field of 1 x 1 matter, Equalus Unitus has the power for adding the result information then if the result is equals_to_one is called by Equalus Unitus and if equals is to Equalus, it can be proved that "*Who is 1 x 1*" is re markedly, Unitus. The name, Unitus is the encounter of the 1 x 1 field matter. Unitus is the pro-study of the thing – The multiplication of one by itself :- 1 x 1 Field Matter.

- The who-ness to who is *1 x 1* needs the pro-study of the thing – The multiplication of one by itself. The 1 x 1 field matter has being proving to be called by Unitus if it encountered. As depicted in the answer to question (6), Equalus Unitus has prove "*Who is 1 x1*" to be Unitus and so the "*Who-ness to Who is 1 x 1?*" is Equalus. The "W*ho-ness to who is 1 x 1?*" is qualified to be handed either to the right or left. To the main question "*Who-ness to who is 1 x 1?*" is Rightus Equalus.

- The difference of one by itself is 1-1. from the theorem (3)

  $1 - 1 = 0.$

This means the result of the difference of one by itself is a subtract of the number, 0. that is the

result is zero.

- The where-ness to what is 1 – 1 is answered by checking where on the hand system, 1 – 1 lies. From the theorem (3)

  $1 - 1 = 0$

  LHS = RHS

  Deductively, on the hand system 1 – 1 is on the left hand side to equals_to_one. The thinking on 1 – 1 on the three systems give the following characteristics :

  (i) It is called Subtractus Unitus.

  (ii) It has the minus sign in the field system.

  (iii)It lies in the left hand side in the hand system.

  (iv) It's number system is comprised of one(1) and zero(0).

2 CLAIMS and RESULTS OF WORK

The following are claims in the understanding of the unification of arithmetical signs:
1 / 1 is the division of one by itself. The which-ness of 1 x 1 is the division of one by itself. 1 x 1 is the multiplication of one by itself. The sign of equality of the result of 1 x 1 from the right hand system is =1. The sign of equality of the result of 1 = 1 from the left hand system is 1x. The characteristics of division equality theorem is made up of 4 parts. 1=1 is a perfect quality of product. A perfect quality product applies the RH-structure, perfection and perfect assignment. The H-O-N system comprises of operator or field system, hand system and number system. The HON is a Z_2 field system. Equalus Unitus is involve in the provision of product information in the 1 x 1 matter. Unitus is the name of the encounter of the 1 x 1 field matter. Subtractus Unitus is the name called in the encounter of 1 – 1 matter.

4 CONCLUSION

The arithmetical signs are unified here in this paper by doing proofs[3]. This is real in the investigation or analysis of the arithmetic equality of sum of ones, substraction of ones, divsion of ones and multiplication of ones. Electronic machine is explained along an arithmetic theorems. Here, I discuss an arithmetic electronics in terms of circuit topology, topological representation of arithmetic operations. Again, furthemore is a physical look on lump

element equivalence of circuit topology of arithmetic operations. The number system is also discussed as a coindot approach in generating many digits for a number. Three approaches were envisaged in consideration to actual implementation. This sort to have an electronic machine implementation of concepts developed in this paper. There is an electronic links to Nanoscale concepts just for intellectual purposes.

Compliance with Ethical Standards:

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Conflict of Interest:

Author, Prof. Frank Appiah declares that he has no conflict of interest .

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