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Power Optimization in High Performance Advanced Micro-Controller Bus Architecture in AHB

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Abstract. AHB which is Advanced High-performance Bus is a high-performance bus in AMBA (Advanced Microcontroller Bus Architecture) based Micro-controller. It is widely used as an interconnection standard for System on Chip (SoC) design. In this paper, we present the design of the AMBA AHB protocol with different modes of operation. The design of the AHB Protocol is developed comprising of the basic blocks such as Master, Slave, Decoder, and Arbiter. This High-performance Bus has a very high speed of data transfer capacity which consumes an enormous amount of power. The power consumption is based on the switching behavior of the clock net. In this work, a technique to reduce the clock net has been developed. All of these operations are developed in Verilog HDL. Modelsim (Simulation tool from Mentor Graphics) is used to simulate the design and X-Power Analyser (Graphical tool for power calculation from Xilinx) is used to calculate power and functional coverage.

Keywords: AMBA-AHB, Dynamic Power, Gated Clock, Negative Latch, SoC

1 Introduction

The AHB (Advanced High Performance) is a high-performance bus in AMBA (Advanced Microcontroller Bus Architecture) family. This AHB can be used in high clock frequency system modules. The AHB act as the high-performance system backbone bus. It allows the easy implementation of different macro functions which perhaps operating at different frequencies (high frequency). The AMBA protocol is technology independent since we implement this standard for any range of operating frequency. It facilitates the right-first-time development of multi-processor designs with large numbers of controllers and peripherals. It is was developed by ARM Ltd in

1996 and the one its trademark. AMBA is used as an on-chip interconnection and management of various functional blocks in a System-on-Chip (SoC). System-on-chip refers to integrating all components of an electronic system into a single integrated circuit (chip). An SoC can include one or more microcontroller, microprocessor and DSP, different Memory components, Sensors, digital and analog signal components, timers, voltage regulators and several other components. SoC is widely used in the designing of embedded systems because there are several advantages like small size, high reliability, low memory requirements, and cost-effectiveness.

2 AMBA AHB Different Components

AMBA Protocol mainly consists of three separate buses. These buses are Advanced high-performance bus (AHB), Advanced system bus (ASB) and Advanced peripheral bus (APB). All of these buses have different tasks and functions. Advanced high-performance bus and ASB is generally used to carry data at high data rate whereas Advanced peripheral bus is used for low peripheral devices which generally work at low speed. Both of these buses are separated by the bridge which generally ensures that there is no communication gap between low peripherals on APB with the high peripheral or high-speed processors on AHB and also ensures that no data loss between AHB to APB or APB to AHB data transfers. [8]

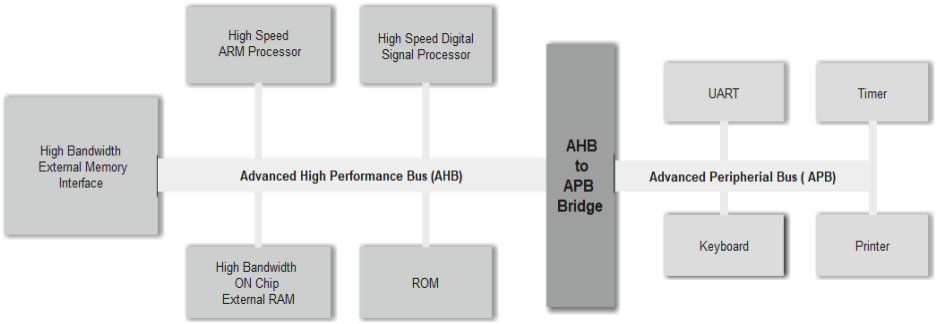


Fig. 1. A Typical AMBA based Micro-controller

AMBA AHB consists of four main parts- AHB Master, AHB Slave, AHB Arbiter, and Decoder. In AMBA AHB there are multiple masters and multiple slaves are available, but at a time one master and one slave can interact. The decoder is used for decoding the address given by the master and relates to the respective slave. The bus is provided by the arbiter to the master for the communication. [7]

1. AHB Master - A master can initiate read and write operations by providing address and control information. As there are multiple master and slaves are available but only one master can communicate or will interact with the one slave only.

2. AHB Slave - A slave performance the operation after getting information from its Master. Here the Read/Write operation is performed which will be given by Master. After completion of the operation, this will give an acknowledge signal back to the master which tells that the operation has been done successfully or get fail.
3. AHB Arbiter - If Master wants to communicate with the slave it first interacts with an arbiter which ensures the availability of a bus for communication. If the bus is free then arbiter grant the request by 'hgrant' signal.
4. Decoder - The decoder is used for decoding the address and information given by master and relates to the respective slave**.**

3 Designing of AMBA AHB

In AMBA AHB there are basically different types of operation for data transfer from master to slave. In Simple Transfer operation there is no wait state hence, 'hready' signal is always low.

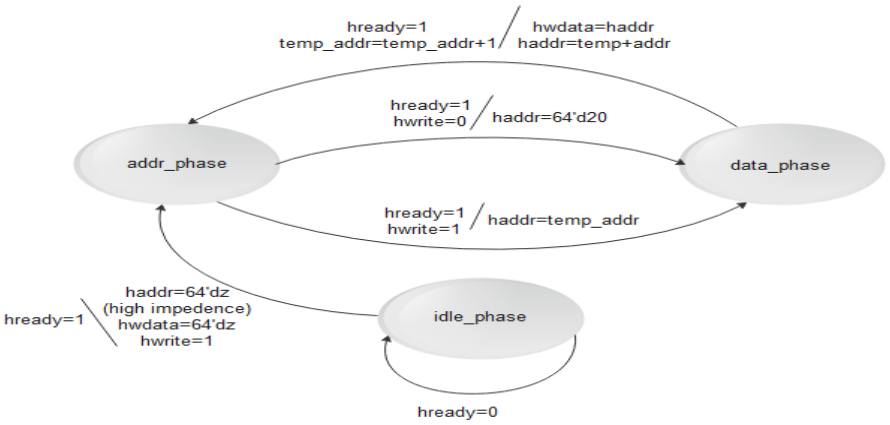


Fig. 2. FSM of Simple Transfer

In wait state transfer operation the presence of low 'hready' signal bring out the transfer operation in wait state hence, whenever when the 'hready' is low, it will go to the wait State.

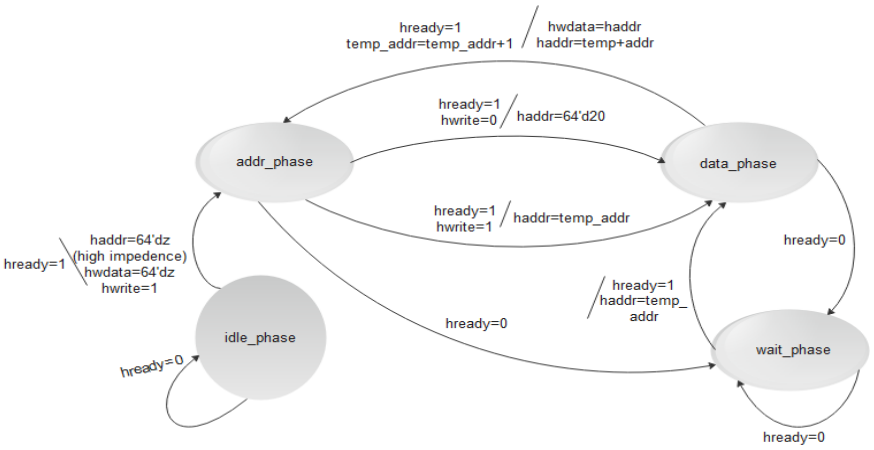


Fig. 3. FSM of Transfer with Wait State

Burst mode operation is used in system-level buses like AHB. It can fetch a large amount of data at a time and then implemented it through the pipelining process. Burst mode eliminated the high impedance state (tri-state) during the transfer of data.

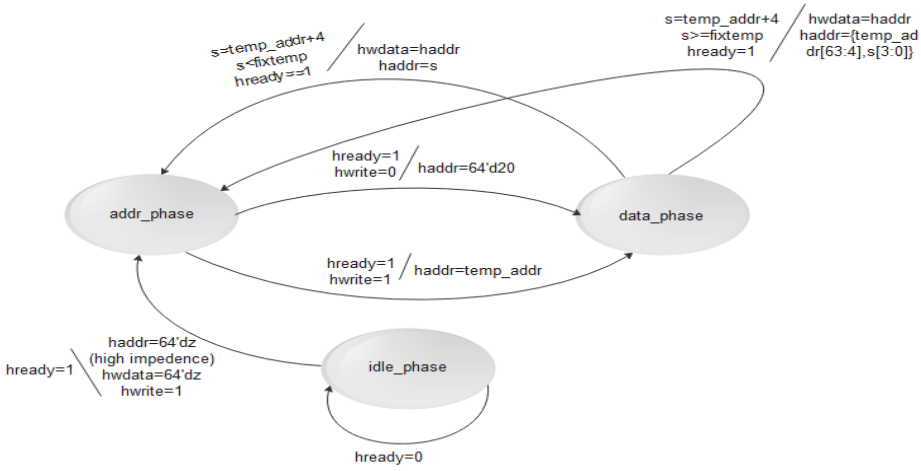


Fig. 4. FSM of Burst Transfer Type Operation

4 High Power Dissipation in AHB Based Micro-controller

The AMBA AHB is a high bandwidth System Bus that carries a date with a high data rate. The performance of the typical AMBA based protocol is just a sequential circuit based on the conventional clock system. The sequential circuits in a system are considered major contributors to the power dissipation since one input of sequential circuits is the clock, which is the only signal that switches all the time. Reduction of switching activity needs analysis of signal transition probabilities, and the other techniques like logic optimization, gated clock, and prevention of glitches. The total switched capacitance can be decreased by clock gating or stop certain blocks from useless switches.

4.1 Low Power Design Principle

Power consumption in any sequential circuit is determined by several factors including frequency f, supply voltage V, data activity α, capacitor C, leakage, short circuit current as

$$P_{dynamic} = \alpha C V_{dd}^2 f \quad [3]$$

$P_{dynamic}$ is also called the switching power and dynamic power. Dynamic power dissipation is only consumed when there is switching activity at any nodes in a CMOS circuit. The dynamic power dissipation is therefore dependent upon the number of times a capacitor is charged and discharged. Hence as the frequency of switching increases so the dynamic power dissipation increases. This charging and discharging of the capacitor is based on number of times clock signal is feed to the circuit.

This switched capacitance can be decreased by clock gating or stop certain blocks from useless switches. Based on the power consumption equation, there are various ways to lower power consumption. Since clocking system is identified as the dominating contributor of the total dynamic power dissipation [3].

4.2 Clock Gating Technique

The clock net is responsible for power dissipation in the synchronized digital circuit. In the clock gating technique, this clock net is reduced. The clock gating is disabled the clock where unwanted switching is not required. In this clock gating technique, we use a negative latch based technique to reduce power. This negative latch based technique is used to reduce power dissipation in the sequential circuit and it is considered as the best technique. [5],[6]

Clock gating logic aims at generating a clock signal by making the clock sensitive to a control signal which allows it to propagate only when the particular functional unit has to be triggered. A control signal has to be generated based on the design considerations. Introduce the enable signal at the design phase when there is a clear

understanding of the various functional blocks in the system. The gated clock, which has a much lesser toggle rate, drives the functional block thus saving a considerable amount of power [2].

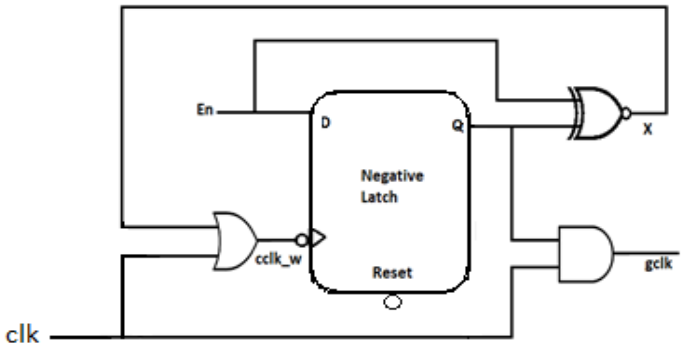


Fig. 5. Negative Latch based Clock gating Technique

5 Simulation and Result Analysis

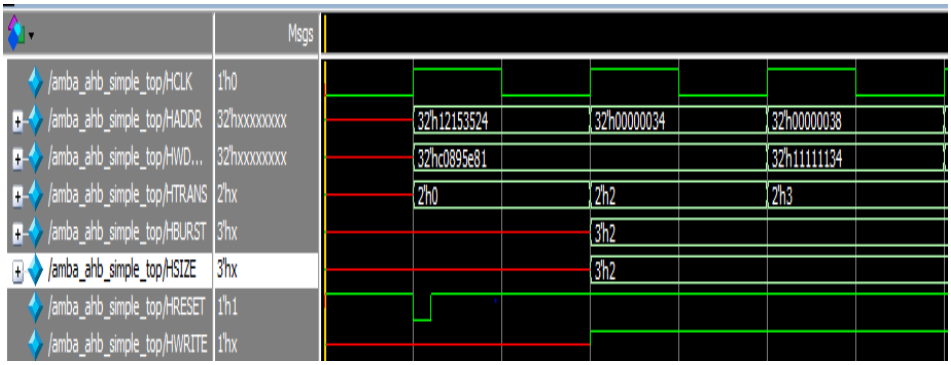


Fig. 6. Simulation of AMBA AHB without Clock gating Technique

In Fig. 6. Use of ‘hready’ signal is to control the number of clock cycles required to complete the transfer. ‘hwrite’ controls the direction of data transfer to or from the master. Therefore, when:

1. When ‘hwrite’ is HIGH, it indicates a write transfer and the master broadcasts data on the write data bus, ‘hwdata’ [31:0]
2. When ‘hwrite’ is LOW, a read transfer is performed and the slave must generate the data on the read data bus, ‘hrdata’ [31:0].

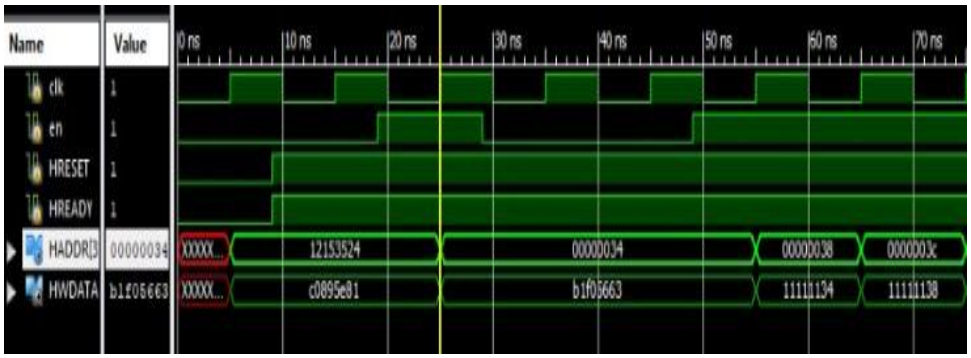
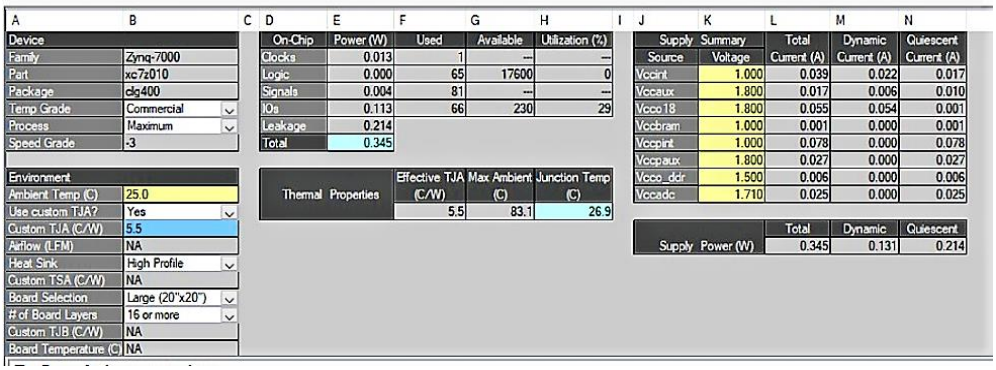


Fig. 7. Simulation of AMBA AHB with Clock gating Technique

In Fig.7. the simulation shows that when the enable 'en' signal is high only then the next data is a change to another state. Until and unless there is no further activity in the System-Bus which results in reducing the unnecessary switching in the System-Bus.



Device	
Family	Zynq-7000
Part	xc7z010
Package	clg400
Temp Grade	Commercial
Process	Maximum
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	Yes
Custom TJA (C/W)	5.5
Airflow (LFM)	NA
Heat Sink	High Profile
Custom TSA (C/W)	NA
Board Selection	Large (20"x20")
# of Board Layers	16 or more
Custom TJB (C/W)	NA
Board Temperature (C)	NA

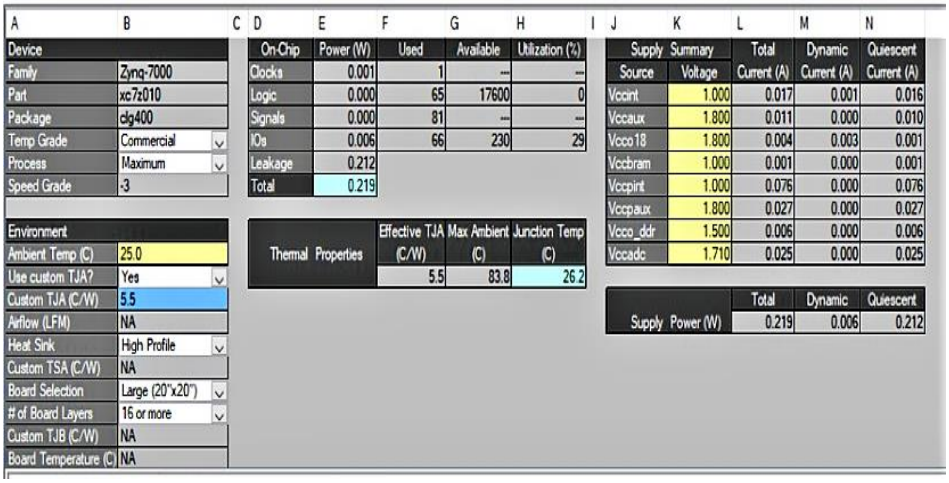
On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.013	1	---	---
Logic	0.000	65	17600	0
Signals	0.004	81	---	---
IOs	0.113	66	230	29
Leakage	0.214			
Total	0.345			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	5.5	83.1	26.9

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.039	0.022	0.017
Vccaux	1.800	0.017	0.006	0.010
Vcco18	1.800	0.055	0.054	0.001
Vccbram	1.000	0.001	0.000	0.001
Vccpint	1.000	0.078	0.000	0.078
Vccpaux	1.800	0.027	0.000	0.027
Vcco_ddr	1.500	0.006	0.000	0.006
Vccadc	1.710	0.025	0.000	0.025

	Total	Dynamic	Quiescent
Supply Power (W)	0.345	0.131	0.214

Fig. 8a. Power analyses of AMBA AHB without clock gating technique



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Heat Sink	High Profile
Custom TSA (C/W)	NA
Board Selection	Large (20"x20")
# of Board Layers	16 or more
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.001	1	---	---
Logic	0.000	65	17600	0
Signals	0.000	81	---	---
IOs	0.006	66	230	29
Leakage	0.212			
Total	0.219			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	5.5	83.8	26.2

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.017	0.001	0.016
Vccaux	1.800	0.011	0.000	0.010
Vcco18	1.800	0.004	0.003	0.001
Vccbram	1.000	0.001	0.000	0.001
Vccpint	1.000	0.076	0.000	0.076
Vccpaux	1.800	0.027	0.000	0.027
Vcco_ddr	1.500	0.006	0.000	0.006
Vccadc	1.710	0.025	0.000	0.025

	Total	Dynamic	Quiescent
Supply Power (W)	0.219	0.006	0.212

Fig. 8b. Power analyses of AMBA AHB with clock gating technique

Fig. 8a. and 8b. illustrate the performance of the proposed clock gated AMBA AHB bus. The result of AMBA AHB system-bus with conventional clock technique is compared with the proposed clock gated AMBA AHB system-bus over the clock frequency of 99 MHz and shows that the power consumption is reduced from 0.345 to 0.219 when the clock system in the system-bus has been changed to negative latch clock gating technique. The power consumption is calculated with the help of the XPower Analyzer tool of Xilinx ISE DESIGN SUIT 14.7a.

6 Conclusion

In this paper, the Advanced Microcontroller Bus Architecture (AMBA) AHB, which is an open System on-Chip bus protocol for high-performance buses on low-power devices is studied and designed successfully and simulated. Also, AHB which consumes more power due to its clock net behavior is shown with and without clock gating respectively and it is found that the power consumption is reduced when we use clock gating instead of a simple clock.

In the present work, we have simulated the AMBA AHB and shows the result in software and in the future, when it will be implemented on the FPGA platform this can be shown more accurate and precise results.

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